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## MULTICHIP MOUNTING CIRCUIT

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[There are no amendments to this patent.]

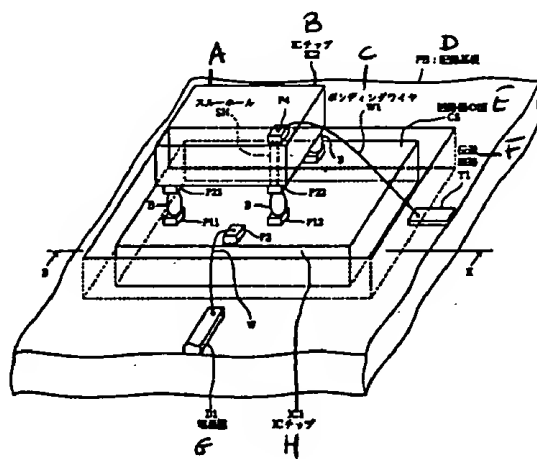
### Abstract

#### Objective

The objective is to provide, in a multichip mounting circuit which composes a circuit by combining a plurality of IC chips, a multichip mounting circuit capable of connecting in state of the waveform degradation, according to impedance miss match being minimal and not having delay in the signal transmission between the IC chips, minimizing the cross wiring when mounting a plurality IC chips, eliminating crosstalk in the intersecting part, and minimizing the mounting area.

# Constitution

Two IC chips are arranged so that the signal terminal of one IC chip opposes the signal terminal of the other IC chip, the mutually opposed signal terminals are mutually connected, a plurality of IC chips are thus superimposed in plural steps, and mutually opposed signal terminals are mutually connected.



- Key: A Through-hole  
 B IC chip  
 C Bonding wire  
 D PB: wiring substrate  
 E Surface on the side of the circuit  
 F Transmission line  
 G Power line  
 H IC chip

Claims

1. A multichip mounting circuit characterized by the fact that in a multichip mounting circuit which composes a circuit by combining a plurality of IC chips,

said two IC chips are arranged so that the signal terminal of one IC chip opposes the signal terminal of the other IC chip, the mutually opposed signal terminals are mutually connected, and along with said plural IC chips being thus superimposed in a plurality of steps, said mutually opposed signal terminals are mutually connected.

2. A multichip mounting circuit characterized by the fact that in Claim 1,

a back surface pad is provided as said signal terminal on the surface opposing the circuit side of said IC chip of above the second step, said circuit side wiring and said back surface pad are connected via a through hole, and the adjacent IC chip or the package lead and said back surface pad are connected according to wire bonding.

3. A multichip mounting circuit characterized by the fact that in Claim 1,

a transmission line is connected to the circuit side surface of said IC chip excluding the IC chip of the uppermost step or the surface opposing said circuit side surface and signal or power is fed to said IC chip one step above via this transmission line.

4. A multichip mounting circuit characterized by the fact that in Claim 1,

a film carrier is interposed between said two IC chips, signals are transmitted and received between said two IC chips

via the wiring on said film carrier, and said adjacent IC chip or adjacent package lead and said two IC chips are connected.

5. A multi-chip mounting circuit characterized by the fact that in Claim 1,

a back surface pad is provided as said signal terminal on the opposite surface from the circuit side of said IC chip of above the second step in case said IC chips are superimposed by more than 3 steps, said back surface pad and the wiring on the circuit side surface of the IC chip of above the second step are connected via a through hole, and the back surface pad of the IC chip of above the second step and the pad of the IC chip positioned in the step above are connected via said through hole.

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